WHAT IS CLAIMED IS:

1. An integrated circuit device, comprising:

a semiconductor substrate;

an isolation layer formed over the semiconductor substrate; and

a layer of silicon material, formed over the isolation layer, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, a second n-type portion contiguous with the second p-type portion, a third p-type portion contiguous with the second n-type portion, and a third n-type portion contiguous with the third p-type portion,

wherein the first, second, and third p-type portions and the first, second, and third n-type portions collectively form a rectifier,

wherein the first p-type portion and the first n-type portion form a cathode of the rectifier, and

wherein the third n-type portion and the third p-type portion form an anode of the rectifier.

2. The integrated circuit device as claimed in claim 1, wherein the second p-type portion is contiguous with the first p-type portion.

3. The integrated circuit device as claimed in claim 1, wherein the third n-type portion is contiguous with the second n-type portion.

4. The integrated circuit device as claimed in claim 1, wherein the second p-type portion includes the first n-type portion and the first p-type portion, each of which being spaced apart from the isolation layer.

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5. The integrated circuit device as claimed in claim 4, wherein the second p-type portion additionally includes a fourth n-type portion spaced apart from the first n-type portion, the first n-type portion and the fourth n-type portion defining a source region and a drain region of an NMOS transistor.

6. The integrated circuit device as claimed in claim 1, wherein the second n-type portion includes the third n-type portion and the third p-type portion, each of which being spaced apart from the isolation layer.

7. The integrated circuit device as claimed in claim 6, wherein the second n-type portion additionally comprises a fourth p-type portion spaced apart from the third p-type portion, the third p-type portion and the fourth p-type portion defining a source region and a drain region of a PMOS transistor.

8. The integrated circuit device as claimed in claim 1, wherein the first n-type portion and the first p-type portion are contiguous with the isolation layer.

9. The integrated circuit device as claimed in claim 8, wherein the second p-type portion includes a fourth n-type portion formed spaced apart from the first n-type portion, and wherein the first n-type portion and the fourth n-type portion define a source region and a drain region of an NMOS transistor.

10. The integrated circuit device as claimed in claim 9, wherein the NMOS transistor comprises a gate for receiving a voltage to turn on the NMOS transistor.

11. The integrated circuit device as claimed in claim 1, wherein the third n-type portion and the third p-type portion are contiguous with the isolation layer.

12. The integrated circuit device as claimed in claim 11, wherein the second n-type portion includes a fourth p-type portion formed spaced apart from the third p-type

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portion, and wherein the third p-type portion and the fourth p-type portion define a source region and a drain region of a PMOS transistor.

13. The integrated circuit device as claimed in claim 12, wherein the PMOS transistor comprises a gate for receiving a voltage to turn on the PMOS.

14. The integrated circuit device as claimed in claim 13, wherein the gate of the PMOS transistor is coupled to the anode of the rectifier.

15. The integrated circuit device as claimed in claim 13, wherein the second p-type portion includes a fourth n-type portion formed spaced apart from the first n-type portion and contiguous with the fourth p-type portion, and wherein the first n-type portion and the fourth n-type portion define a source region and a drain region of an NMOS transistor.

16. The integrated circuit device as claimed in claim 1, further comprising at least one isolation portion formed contiguous with the rectifier.

17. An integrated circuit device, comprising:

a semiconductor substrate;

an isolation layer formed over the semiconductor substrate;

an n-type MOS transistor having a gate, a drain region, and a source region formed over the isolation layer; and

a p-type MOS transistor having a gate, a drain region, and a source region formed over the isolation layer and contiguous with the n-type MOS transistor, wherein the n-type MOS transistor and the p-type MOS transistor form a rectifier to provide electrostatic discharge protection.

18. The integrated circuit device as claimed in claim 17 further comprising an electrostatic discharge circuit for providing the bias voltage to trigger the rectifier, the electrostatic discharge circuit comprising a first inverter including a first PMOS transistor having a gate, a source region and a drain region, and a first NMOS transistor having a gate, a source region and a drain region, wherein the gate of the first PMOS transistor is coupled to the gate of the first NMOS transistor, and the gate of the p-type MOS transistor is coupled to the drain region of the first PMOS transistor and the drain region of the first NMOS transistor.

19. The integrated circuit device as claimed in claim 18, wherein the gate of the p-type MOS transistor is coupled to receive the bias voltage to trigger the rectifier to provide electrostatic discharge protection.

20. The integrated circuit device as claimed in claim 18, wherein the electrostatic discharge circuit further comprises a second inverter, including a second PMOS transistor having a gate, a source region and a drain region, and a second NMOS transistor having a gate, a source region and a drain region, wherein the gate of the second PMOS transistor is coupled to the gate of the second NMOS transistor, and the gate of the n-type MOS transistor is coupled to the drain region of the second PMOS transistor and the drain region of the second NMOS transistor.

21. The integrated circuit device as claimed in claim 18, wherein the source region of the first NMOS transistor is coupled to ground.

22. The integrated circuit device as claimed in claim 20, wherein the source region of the second NMOS transistor is coupled to ground.

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23. The integrated circuit device as claimed in claim 18, wherein the source region of the first PMOS transistor is coupled to a pad to receive an electrostatic current.

24. The integrated circuit device as claimed in claim 20, wherein the source region of the second PMOS transistor is coupled to a pad to receive an electrostatic current.

25. The integrated circuit device as claimed in claim 17 further comprising a first n-type region, wherein one of the source region and the drain region of the p-type MOS transistor and the first n-type region form an anode of the rectifier.

26. The integrated circuit device as claimed in claim 17 further comprising an electrostatic discharge circuit for providing the bias voltage to trigger the rectifier, the electrostatic discharge circuit comprising a first inverter including a first PMOS transistor having a gate, a source region and a drain region, and a first NMOS transistor having a gate, a source region and a drain region, wherein the gate of the first PMOS transistor is coupled to the gate of the first NMOS transistor, and the gate of the n-type MOS transistor is coupled to the drain region of the first PMOS transistor and the drain region of the first NMOS transistor.

27. The integrated circuit device as claimed in claim 26, wherein the anode of the rectifier is coupled to the gate of the p-type MOS transistor.

28. The integrated circuit device as claimed in claim 26, wherein the gate of the first NMOS transistor and the gate of the first PMOS transistor are coupled in parallel to a resistor and a capacitor.

29. The integrated circuit device as claimed in claim 25, wherein the anode of the rectifier is coupled to a pad to receive an electrostatic current.

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30. The integrated circuit device as claimed in claim 17, further comprising an electrostatic discharge circuit for providing a bias voltage to trigger the rectifier to provide electrostatic discharge protection, wherein the gate of the n-type MOS transistor is coupled to receive the bias voltage

31. The integrated circuit device as claimed in claim 17 further comprising a first p-type region, wherein one of the source region and the drain region of the n-type MOS transistor and the first p-type region form a cathode of the rectifier.

32. The integrated circuit device as claimed in claim 29, wherein the cathode is coupled to at least one diode to prevent the rectifier from being triggered in a non-ESD operation.

33. A method for protecting a silicon-on-insulator semiconductor circuit from electrostatic discharge, comprising:

providing an n-type MOS transistor having a source region and a drain region in the silicon-on-insulator circuit;

providing a p-type MOS transistor having a source region and a drain region, the p-type MOS transistor being contiguous with the n-type MOS transistor;

providing a p-type region contiguous with one of the source region and the drain region of the n-type MOS transistor to form a cathode; and

providing an n-type region contiguous with one of the source region and the drain region of the p-type MOS transistor to form an anode, wherein the n-type region, the p-type region, the p-type MOS transistor and the n-type MOS transistor form a rectifier.

34. The method as claimed in claim 31 further comprising a step of biasing the p-type MOS transistor to trigger the rectifier.

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35. The method as claimed in claim 31 further comprising a step of biasing the n-type MOS transistor to trigger the rectifier.

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